Modeling SI/PI and EMC Problems Through Data: Deterministic, Parametric, and Stochastic Perspectives – Part 1

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One example: Power Integrity

A Power Delivery Network

~50 cm — 8 orders of magnitude — 5 nm

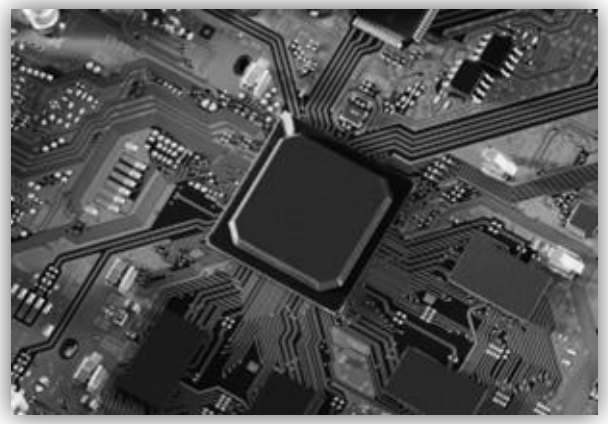
Feature size

Modeling challenges:

multiscale, huge complexity, heterogeneous, interconnected, linear?

Building individual (linear) models: Vector Fitting

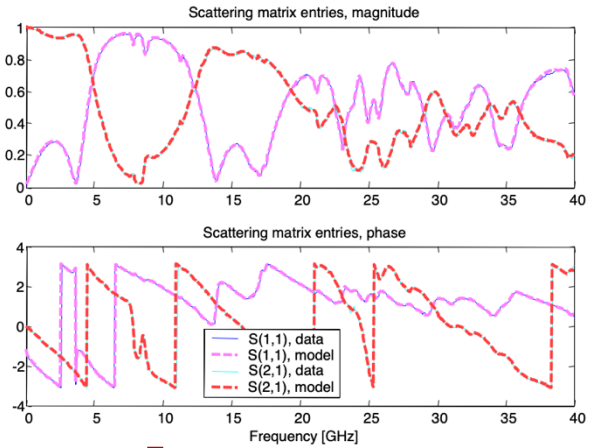
Geometry, materials



Board

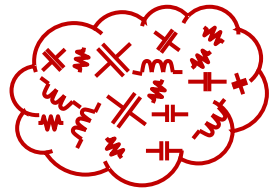
Extraction
EM simulation
Ckt simulation

Scattering data $\hat{S}_k = \hat{S}(j\omega_k)$



Macromodel

$$\dot{x} = Ax + Bu$$
$$y = Cx + Du$$



Rational fitting
Passivity enforcement

Realization
or synthesis

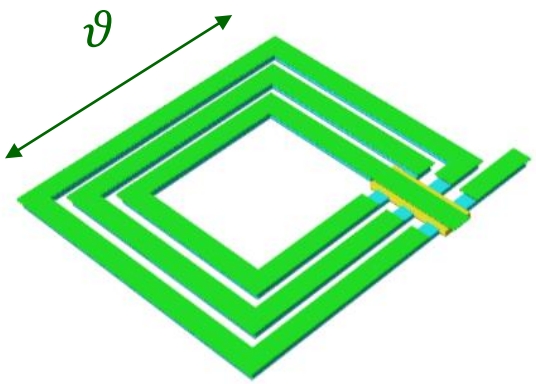
$$S(s) = R_0 + \sum_{i=1}^{\nu} \frac{R_i}{s - p_i}$$

S. Grivet-Talocia, B. Gustavsen, “Passive Macromodeling: Theory and Applications”, New York: John Wiley & Sons, 2016

Linear macromodeling is now a commodity

- Theory and algorithms are available and mature
  - Many improvements documented (2000 – 2026 and counting…)
- Dedicated tools available
  - Including **IdEM** from our own Spinoff (now part of CST/Dassault software)
  - Including proprietary implementations in CAD tool suites
    - Agilent, Ansys, Cadence, CST/Dassault (in alphabetical order) … you name it …
- Recent developments and extensions @ PoliTO
  - Extension to higher complexity
    a) Adding additional variables or parameters: multivariate macromodeling
    b) Extending the number of I/O ports: fast algorithms
  - Extension in scope and application
    c) Nonlinear devices: linearized (voltage regulators), including dynamic small-signal
    d) Model Order Reduction for full Power Delivery Networks
    e) Direct identification of nonlinear macromodels from port responses

a) Multivariate (parameterized) macromodeling



Parametric sweep

Simulation or Measurement

IN

.snp

Multiple S-parameters

$$\breve{\mathbf{H}}_{k;m} = \breve{\mathbf{H}}(j\omega_k;\vartheta_m)$$
$$k = 1,\dots,K;\ m = 1,\dots,M$$

Multivariate Rational Fitting

Stability & Passivity

$$\mathbf{H}(s;\boldsymbol{\vartheta}) = \frac{\mathbf{N}(s;\boldsymbol{\vartheta})}{\mathrm{D}(s;\boldsymbol{\vartheta})}$$

Parameterized model

State-space realization

Circuit synthesis

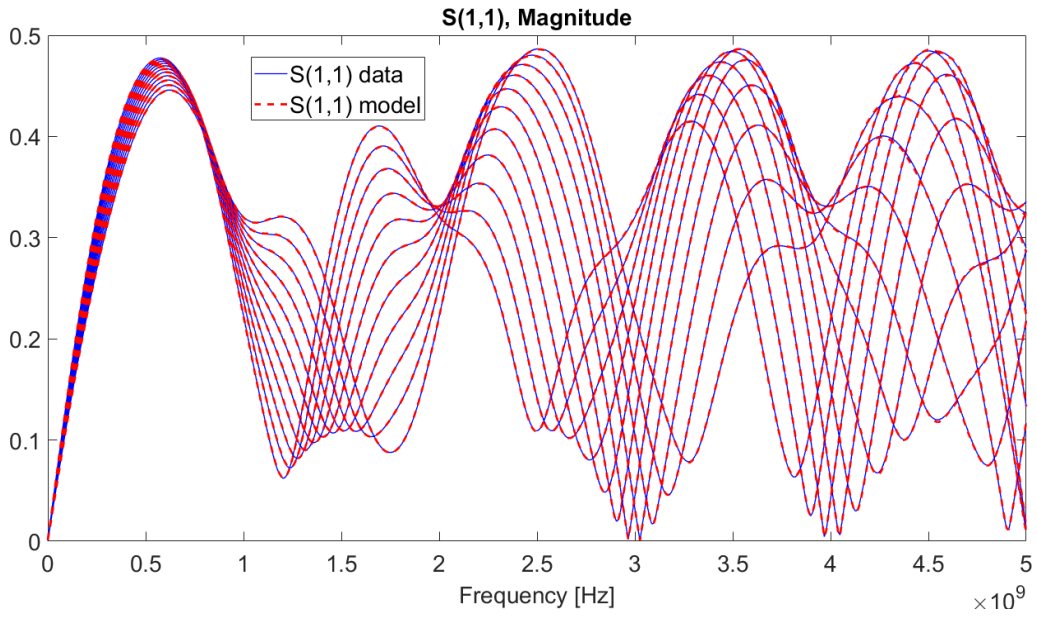
$$\dot{\boldsymbol{w}} = \boldsymbol{A}(\boldsymbol{\vartheta})\boldsymbol{w} + \boldsymbol{B}(\boldsymbol{\vartheta})\boldsymbol{u}$$
$$\boldsymbol{y} = \boldsymbol{C}(\boldsymbol{\vartheta})\boldsymbol{w} + \boldsymbol{D}(\boldsymbol{\vartheta})\boldsymbol{u}$$

OUT

Parameterized SPICE netlist

a) Multivariate (parameterized) macromodeling

Accurate, stable, passive. Guaranteed.



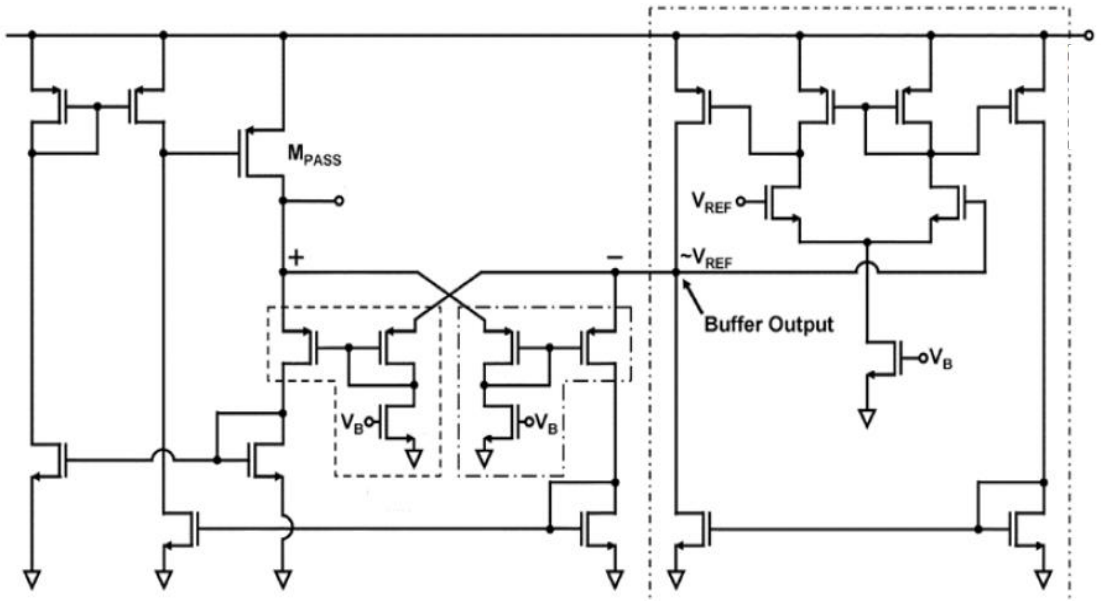
Example: 8-port coupled interconnect

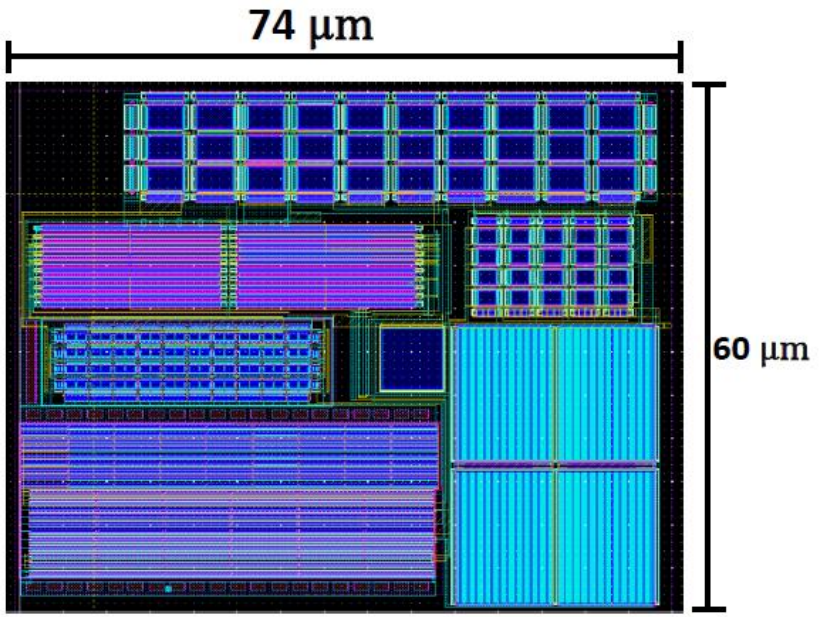
- Single behavioral model
  - SPICE compatible
  - Runs in time or frequency domain
- Dependence on multiple parameters
- Can be used for
  - Building component libraries
  - Sensitivity
  - Design centering and optimization
  - Fast MonteCarlo
- Modeling tool available (w GUI)

→ See Industry Talk 7 by Arne Schröder and Tommaso Bradde for an application

T. Bradde, S. Grivet-Talocia, A. Zanco, and G. C. Calafiore, “Data-driven extraction of uniformly stable and passive parameterized macromodels,” IEEE Access, vol. 10, pp. 15786–15804, 2022.

c) Nonlinear Devices – small-signal





LDO Features	Description	
Tech [nm]	CMOS node	40
V_{DD} [V]	Supply Voltage	1.1
$V_{REF} \approx V_{OUT}$ [V]	Regulated output	0.6
I_{LOAD_MAX} [mA]	Maximum current	10
I_Q [nA]	Quiescent current	138
T_R [µs]	Recovered Time	≈18
C_L [pF]	Load Capacitance	100

Case study: post-layout LDO Voltage Regulator

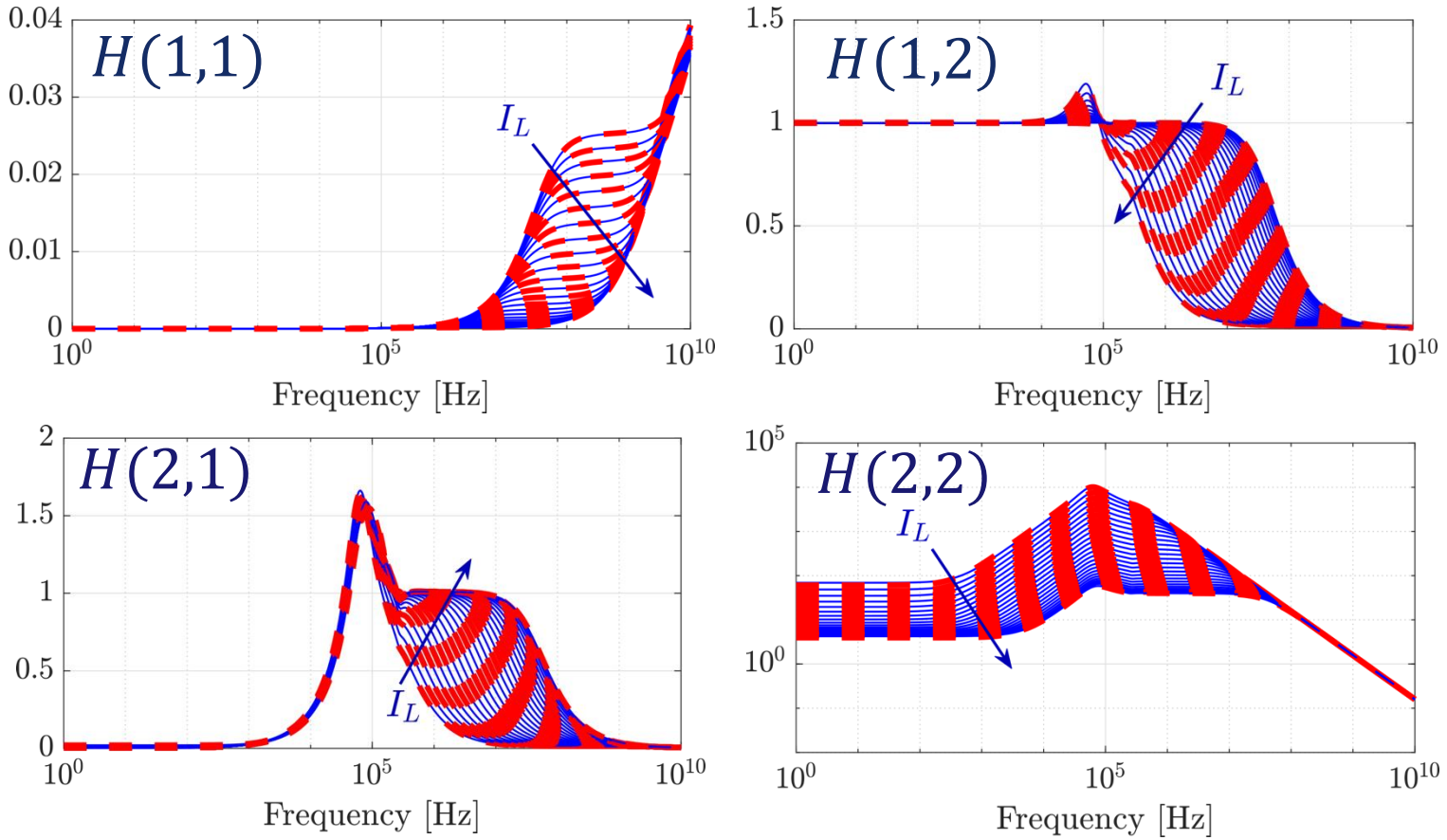
Parameters: supply voltage V_{DD} and output current I_L

c) Small-signal model ($\mathbf{V_{DD}} = \mathbf{1}V$)

Dynamic order: 9

Parameter Dependent Basis: Chebychev Polynomials of order 4 and 3 for numerator and denominator respectively

208 AC responses were exploited for fitting



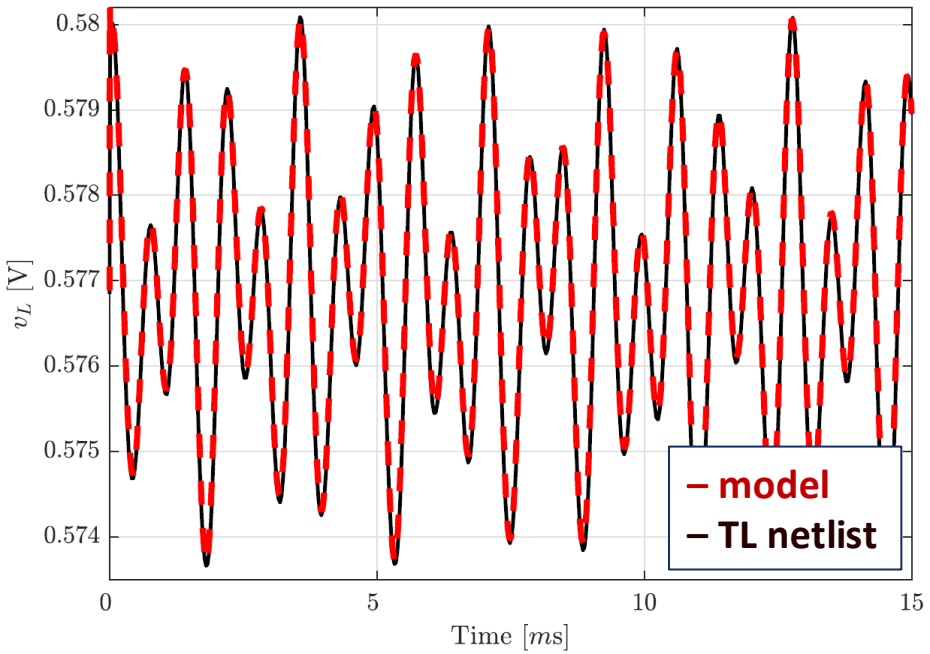
Dashed Red Lines : Model Blue Lines: AC sweep data

c) Transient Simulation: super-fast

Bias point: $V_{DD} = 1V,\ I_L = 5mA$ Computed time span: $100ms$

Small-signal: multitone noise of amplitude $120mV$ overimposed to V_{DD}

Regulated Voltage



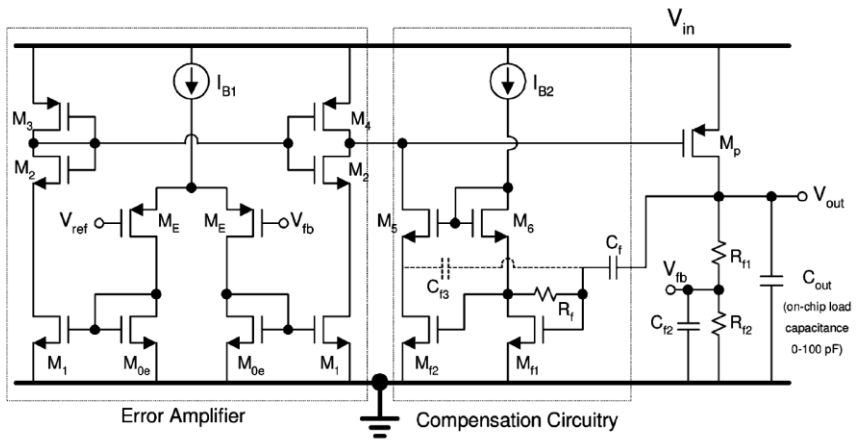
CPU time for transient simulation:

- Behavioral model: 363 ms
- Transistor level post-layout: 258 s

SPEED UP FACTOR: 700X

T. Bradde, S. Grivet-Talocia, et al., "Fast simulation of analog circuit blocks under nonstationary operating conditions," IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 11, pp. 1355– 1368, Sept. 2021.

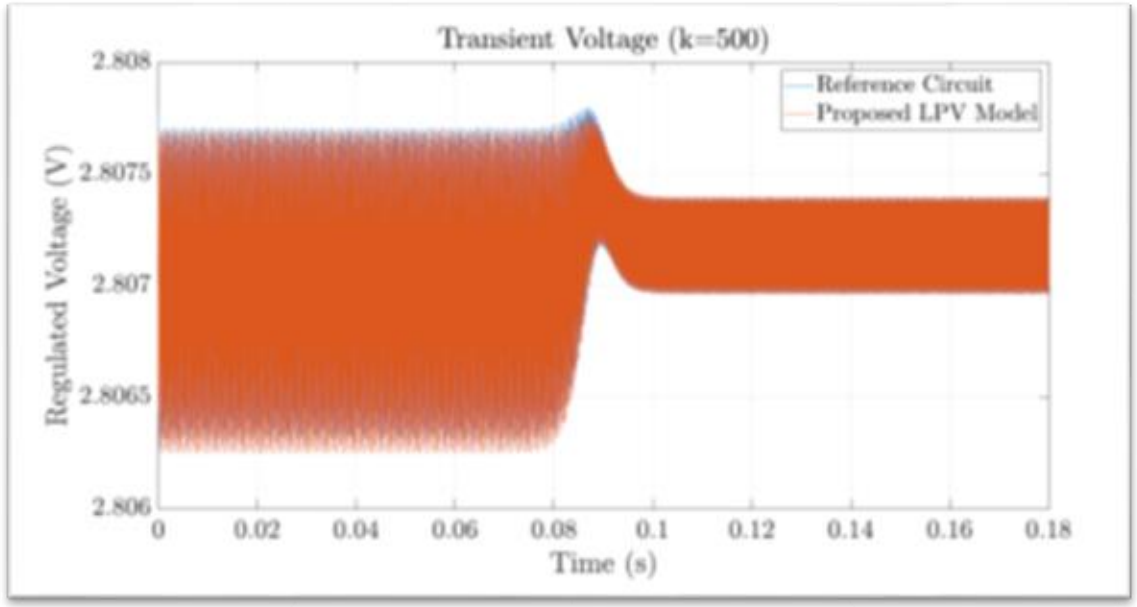
c) Dynamic small-signal: operating point changes!



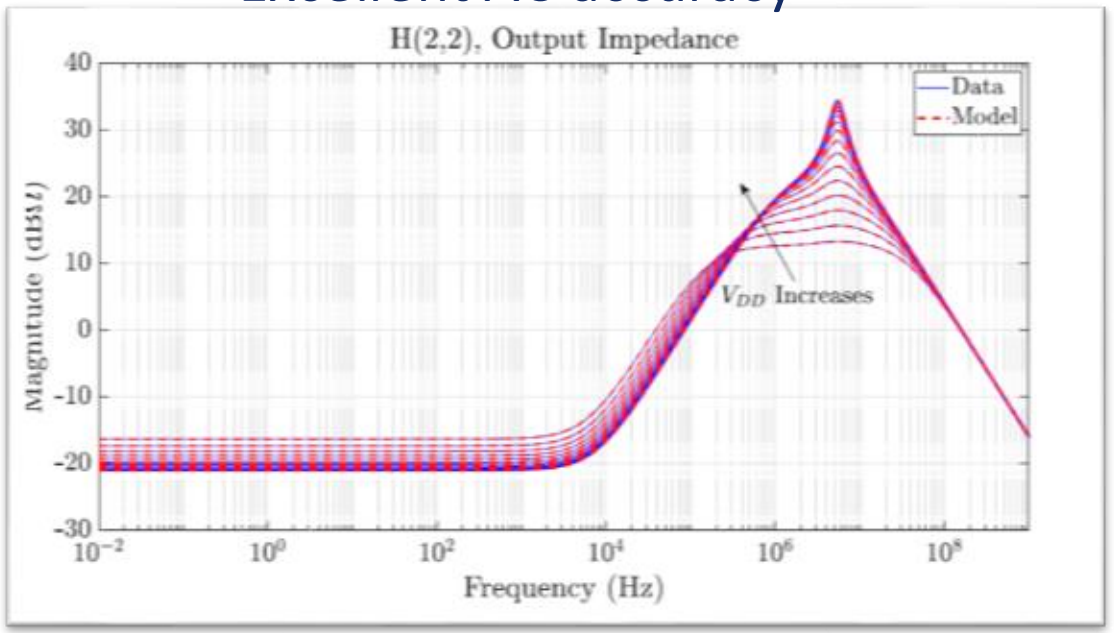
$V_{DD} \in [2.85, 3]$ V

$$\dot{x} = A(U_0(t))x + B(U_0(t))u$$
$$y = C(U_0(t))x + D(U_0(t))u + Y_c(U_0(t))$$

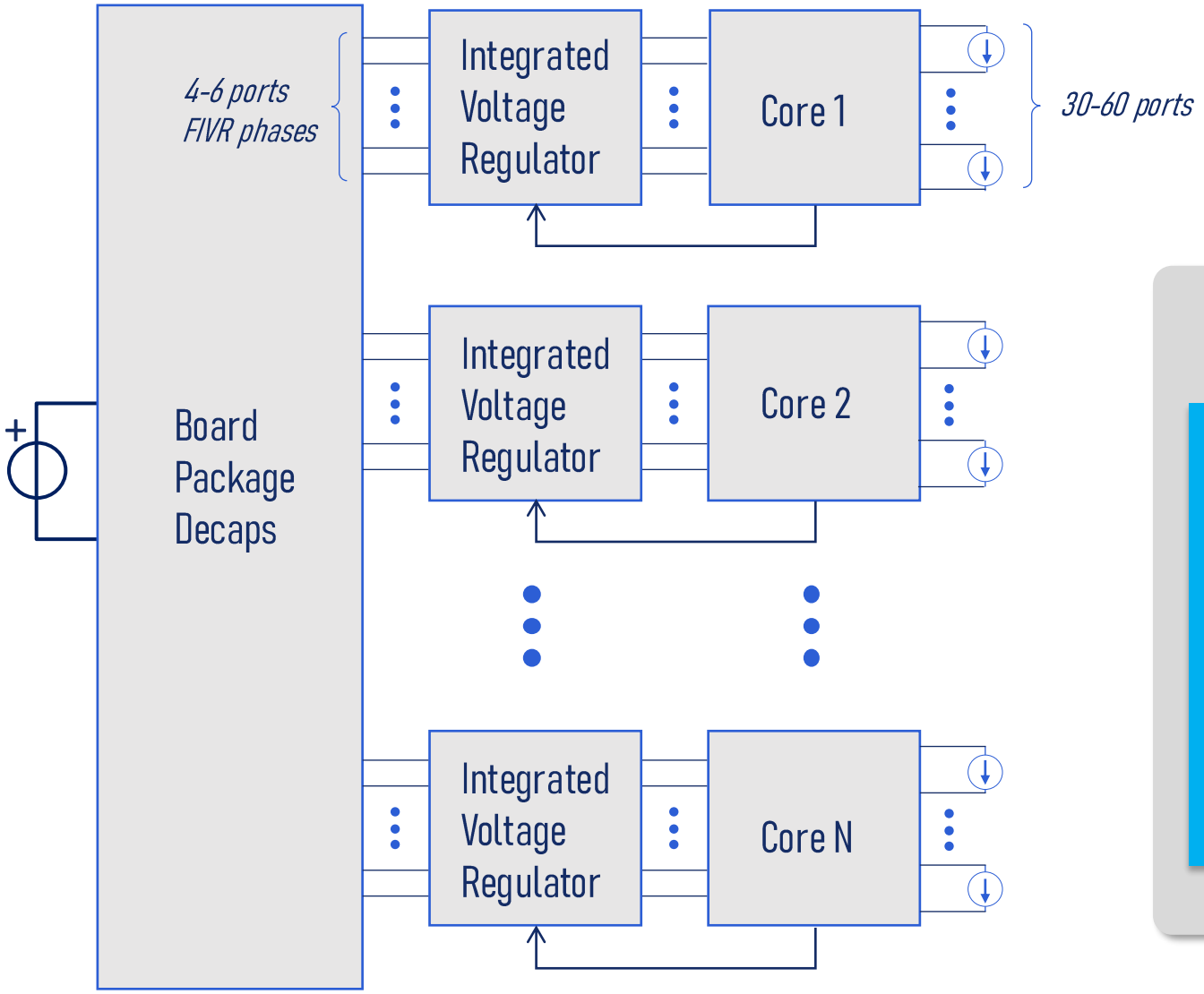
Correct transient response



Excellent AC accuracy



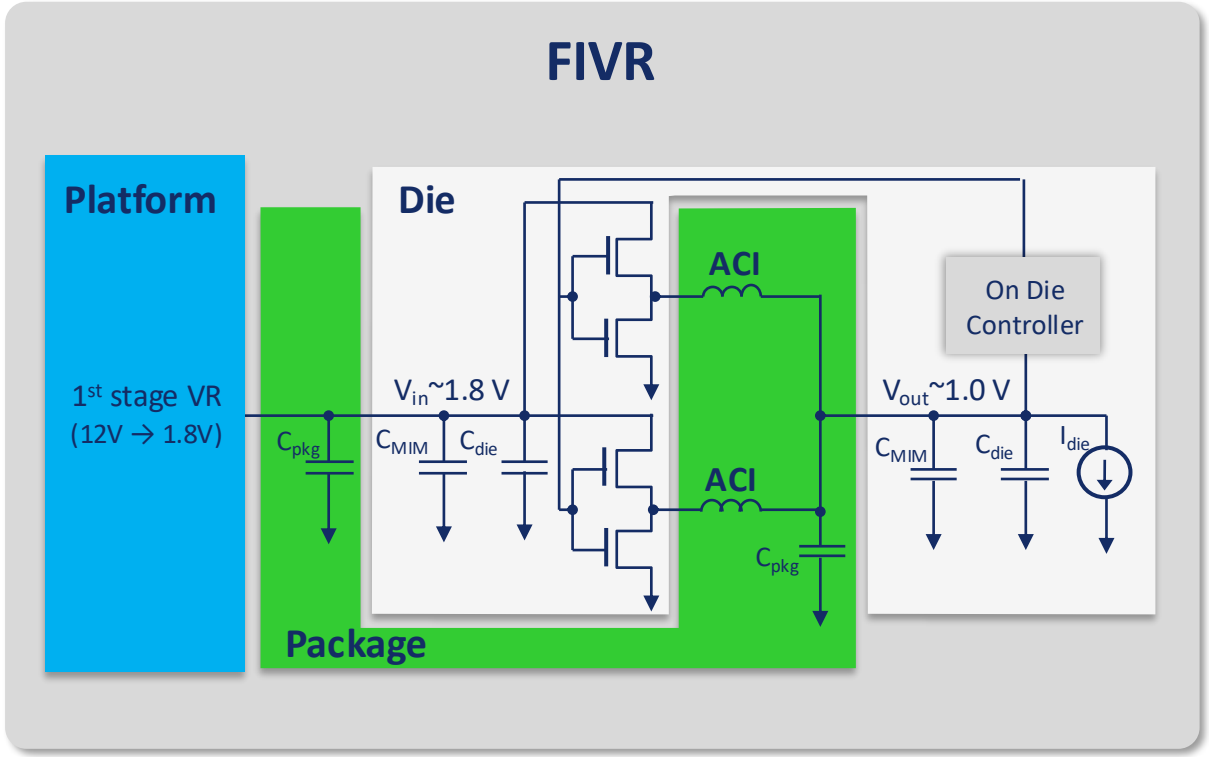
d) MOR for full Power Delivery Networks (with IVR)



Multiphase buck converters

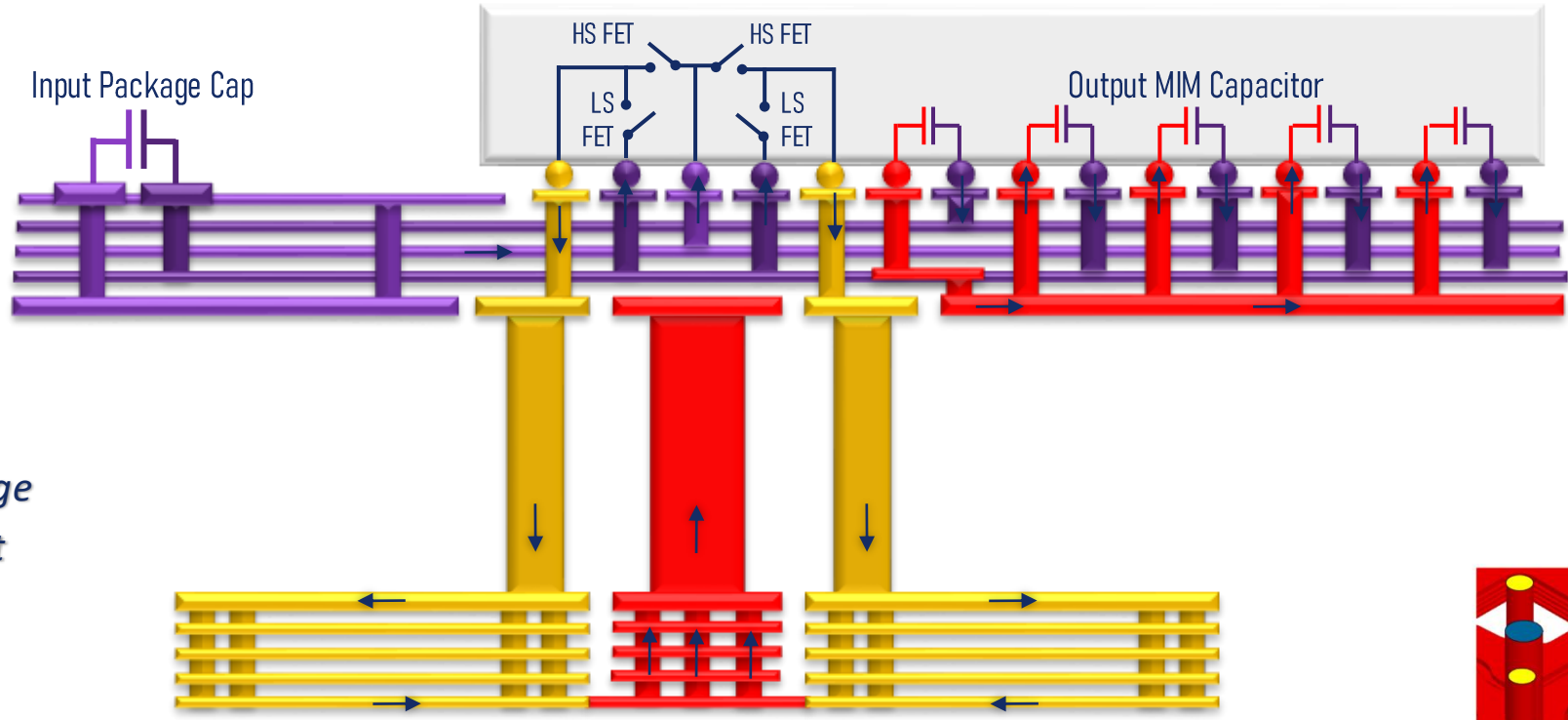
At the chip-package interface

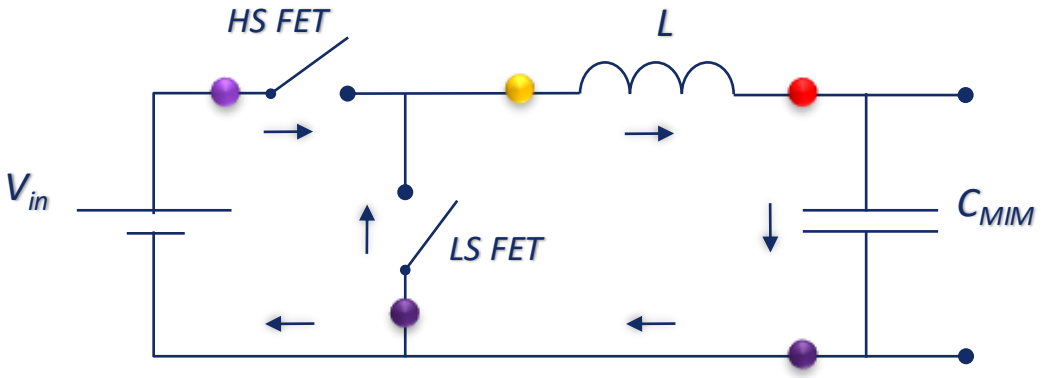
One for each CPU core



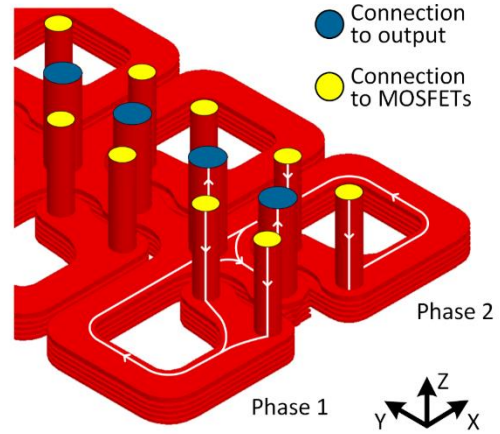
Courtesy: Kaladhar Radhakrishnan, Intel

d) MOR for full Power Delivery Networks (with IVR)





ACI – 3D View

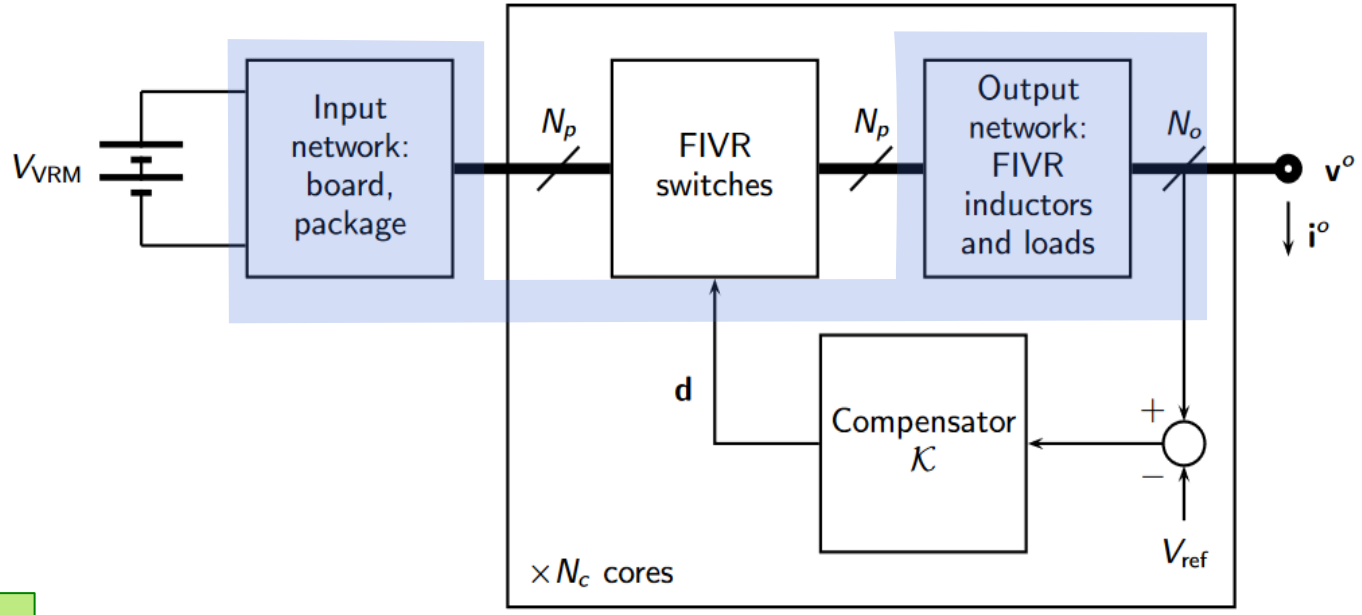


Courtesy: Kaladhar Radhakrishnan, Intel

d) MOR for full Power Delivery Networks (with IVR)

Collect all LTI blocks

$$\begin{cases} E\,\dot{x} = A\,x + B\,u \\ y = C\,x + D\,u \end{cases}$$



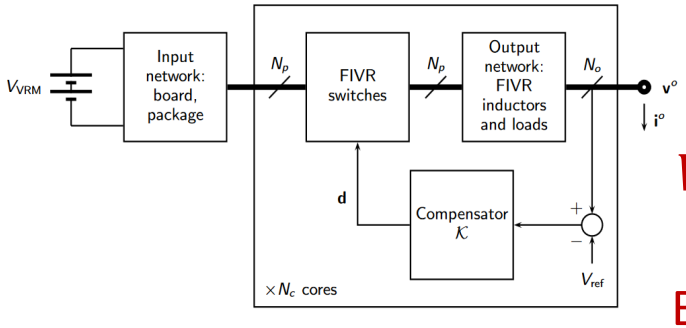
Petrov-Galerkin projection

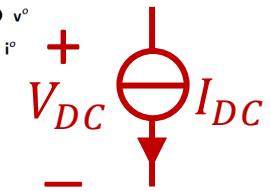
$$\hat{A} = W^T A V$$

Typical compression ratio ~ 100: 1

A. Carlucci, S. Grivet-Talocia, S. Kulasekaran, and K. Radhakrishnan, "Structured model order reduction of system-level power delivery networks," IEEE Access, vol. 12, pp. 18198–18214, 2024.

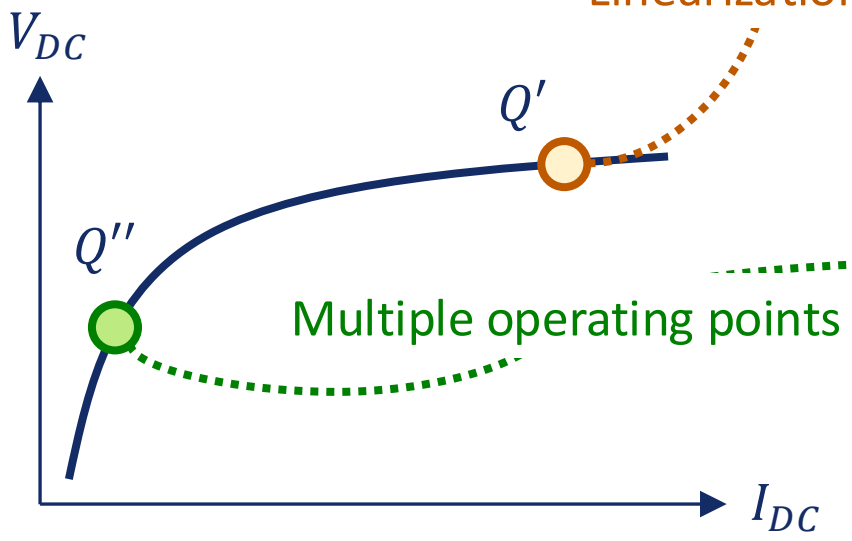
d) MOR for full Power Delivery Networks (with IVR)



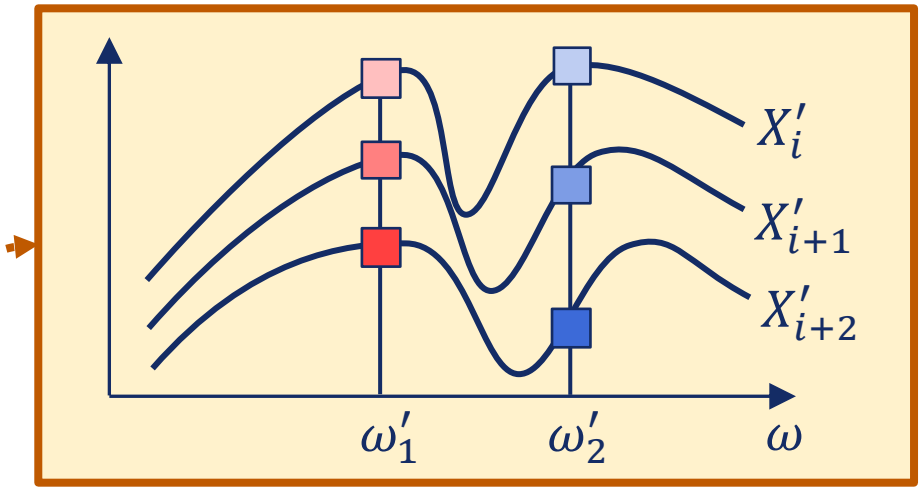


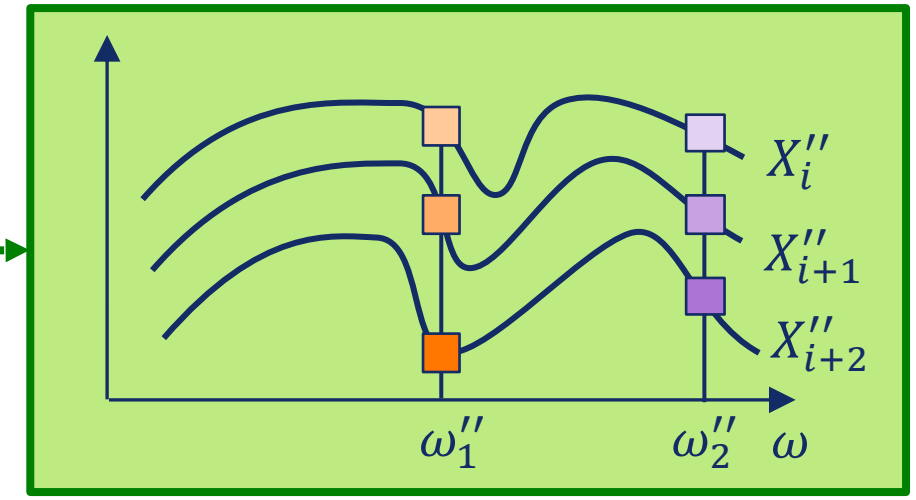
Biasing

Linearization



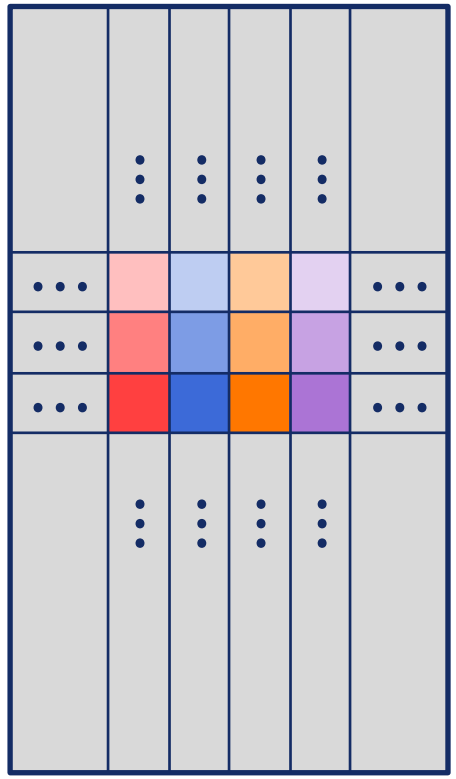
Multiple operating points





Small-signal state responses

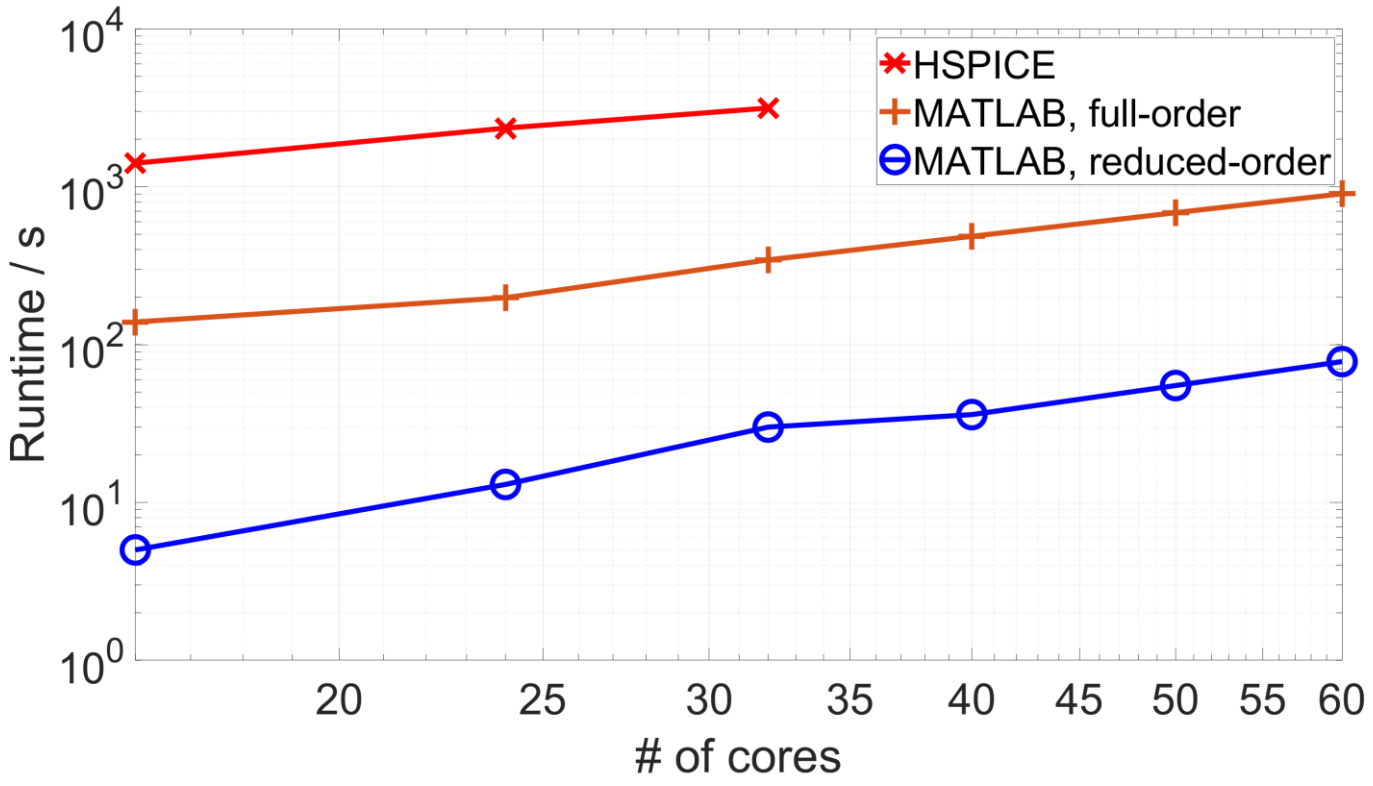
Projection matrix V

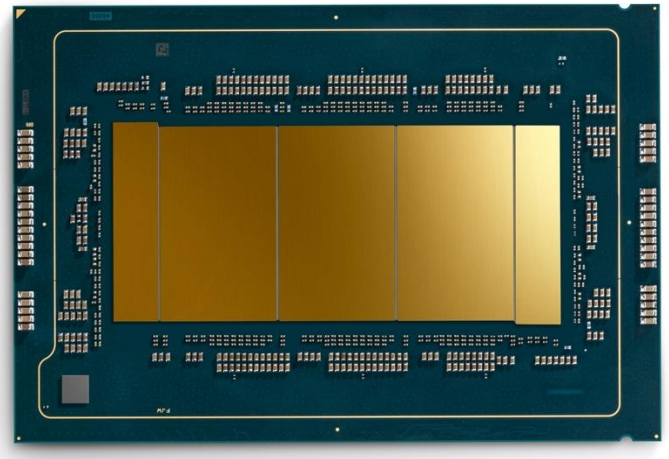


d) MOR for full Power Delivery Networks (with IVR)

HSPICE fails here!

Speedup
$10^2 - 10^3$





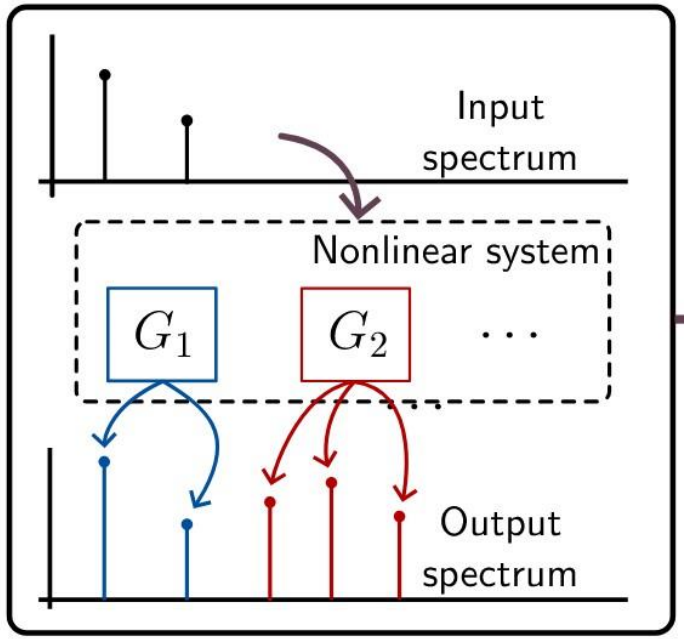
6th generation Intel Xeon processor (2024)

A. Carlucci, S. Grivet-Talocia, S. Kulasekaran, and K. Radhakrishnan, "Structured model order reduction of system-level power delivery networks," IEEE Access, vol. 12, pp. 18198–18214, 2024.

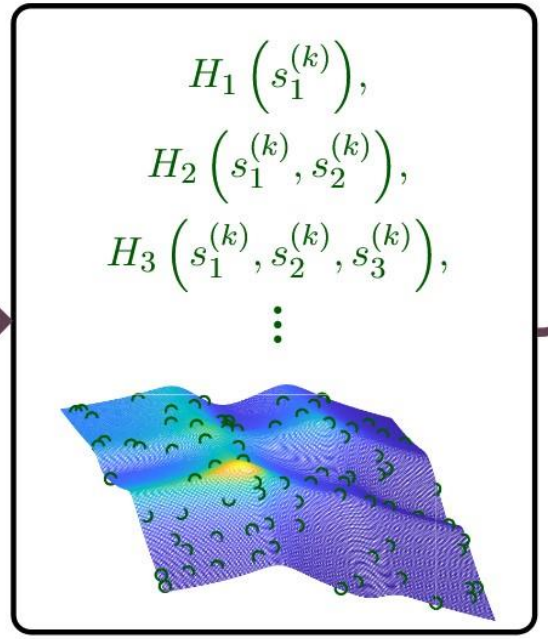
e) Black-box nonlinear macromodeling

Vector Fitting algorithm can be extended to build nonlinear macromodels → See poster!

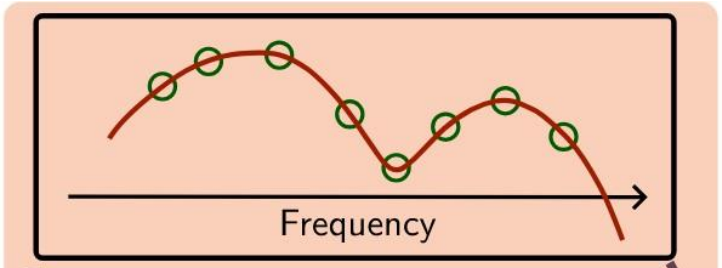
Freq-domain experiments → **Generalized Transfer Function samples** → **Multivariate Rational Fitting**



Nonlinear behavior in harmonic steady-state



Generalized transfer function samples



Multivariate rational model fitting

State-space realization

$$\begin{cases} \dot{\boldsymbol{x}} = \mathbf{A}\boldsymbol{x} + \mathbf{N}\boldsymbol{x}u + \mathbf{B}u \\ y = \mathbf{C}\boldsymbol{x} \end{cases}$$

Bilinear model

SPICE netlist

e) Volterra series theory

Linear I/O behavior: output waveform $y(t)$ related to input excitation $u(t)$:

$$y(t) = \int_0^t h(t-\tau)u(\tau)d\tau$$

Impulse Response $h(t)$ → Transfer Function $H(s)$

Laplace transform

Nonlinear I/O behavior: Volterra series, superposition of nonlinear components

Linear approximation — Quadratic component

$$y(t) = \int_0^t h_1(t-\tau_1)u(\tau_1)d\tau_1 + \iint_0^t h_2(t-\tau_1, t-\tau_2)u(\tau_1)u(\tau_2)d\tau_1 d\tau_2 +$$

$$+ \iiint_0^t h_3(t-\tau_1, t-\tau_2, t-\tau_3)u(\tau_1)u(\tau_2)u(\tau_3)d\tau_1 d\tau_2 d\tau_3 + \ \ldots$$

Cubic component

e) Generalized Transfer Functions

Volterra kernels		Generalized Transfer Functions (GTFs)
$h_1(t_1)$	➡	$H_1(s_1)$
$h_2(t_1, t_2)$	➡	$H_2(s_1, s_2)$
$h_3(t_1, t_2, t_3)$	➡	$H_3(s_1, s_2, s_3)$

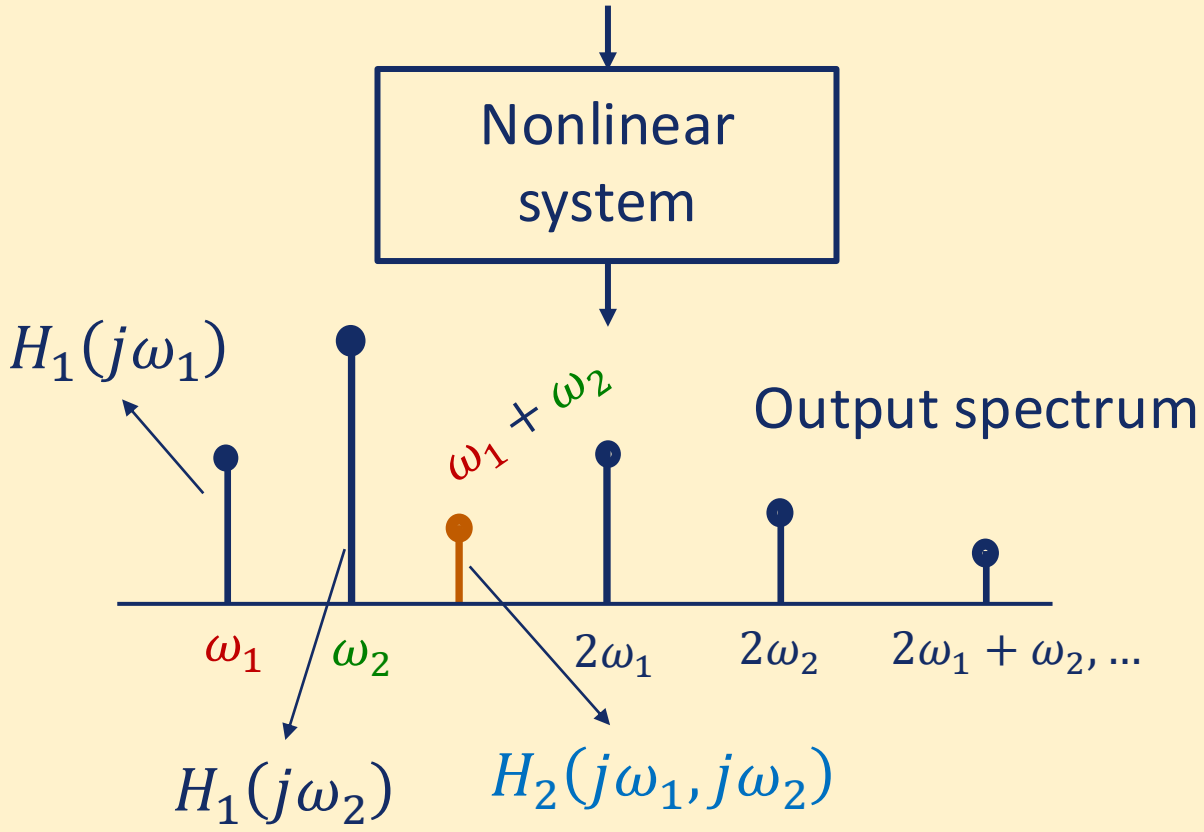
Laplace transform

⋮

A **weakly nonlinear system** is accurately represented by a **small nonlinear degree** (**GTF**s up to H_2, H_3)

Data collection: Harmonic Balance (HB) analysis

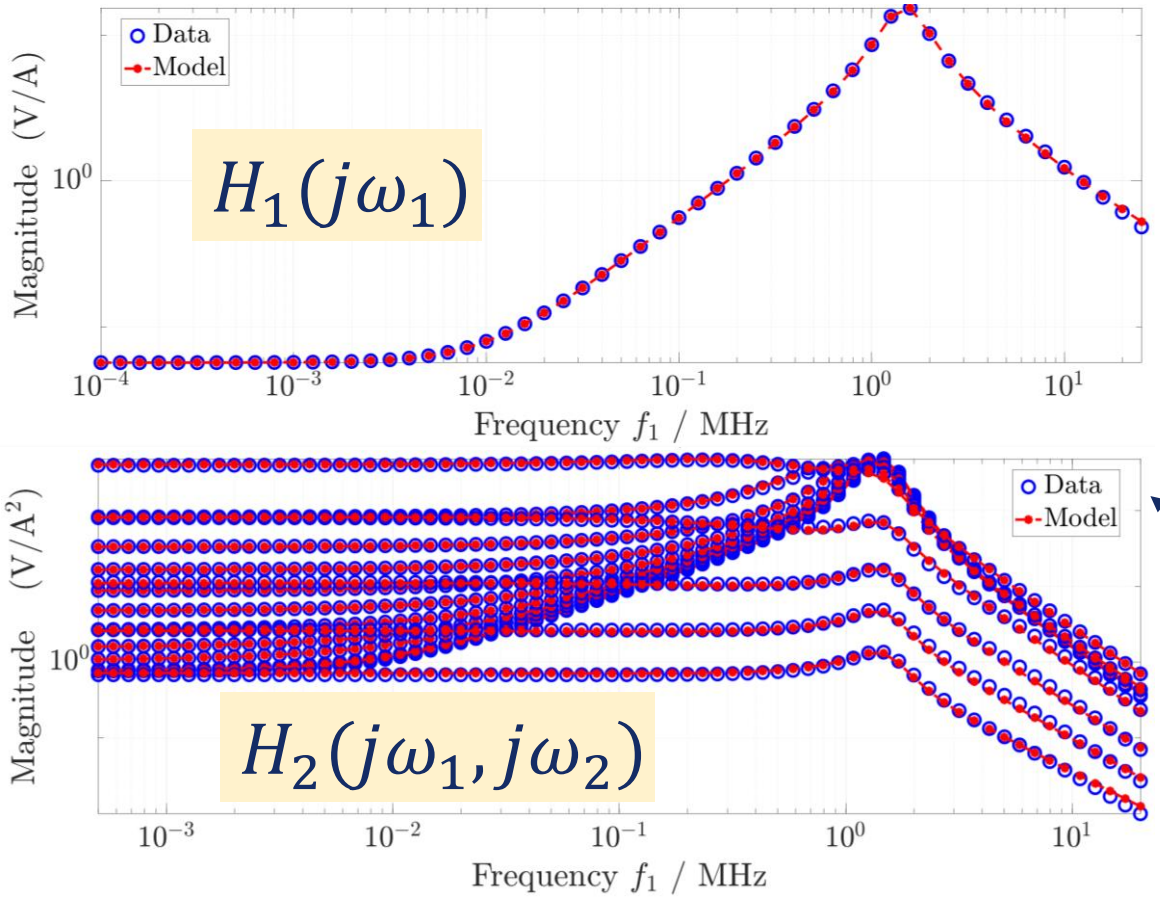
$$u(t) = \alpha \sin \omega_1 t + \alpha \sin \omega_2 t$$

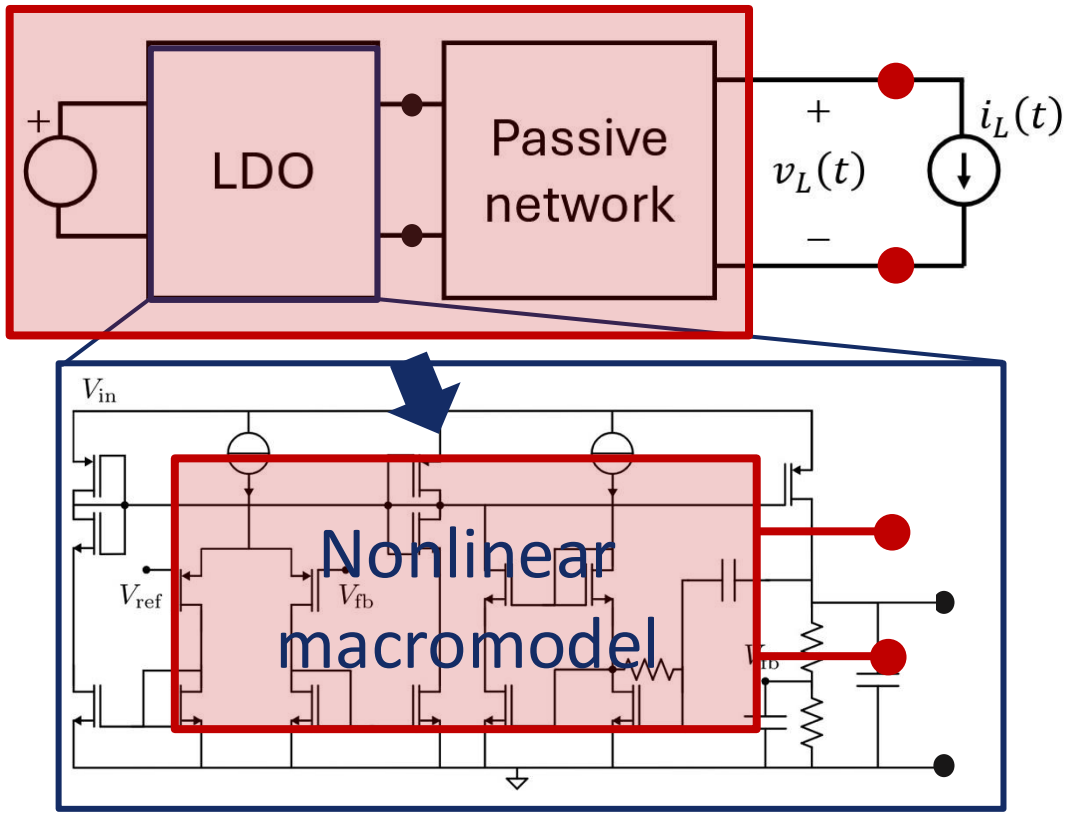


e) Example: LDO regulator

LDO regulator on a PCB

- Model of the output impedance: load voltage response $v_L(t)$ to current $i_L(t)$





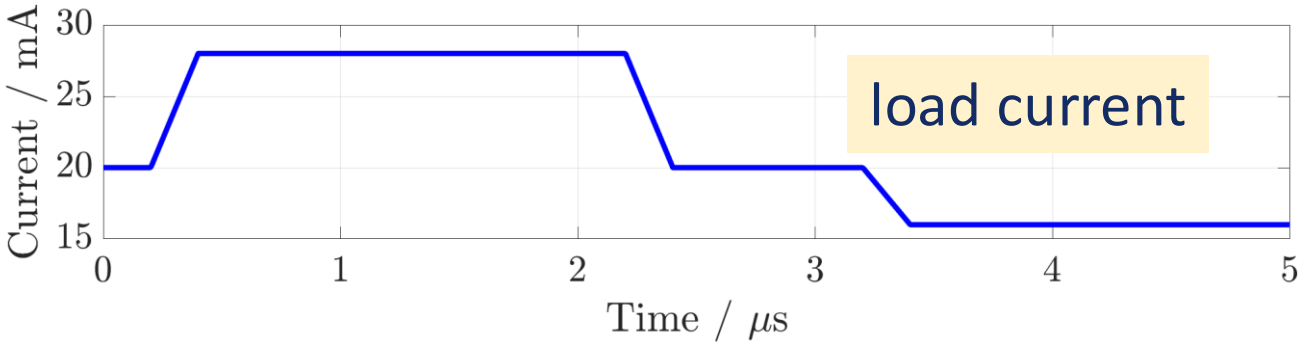
Frequency-domain data from HSPICE's **HB analysis**

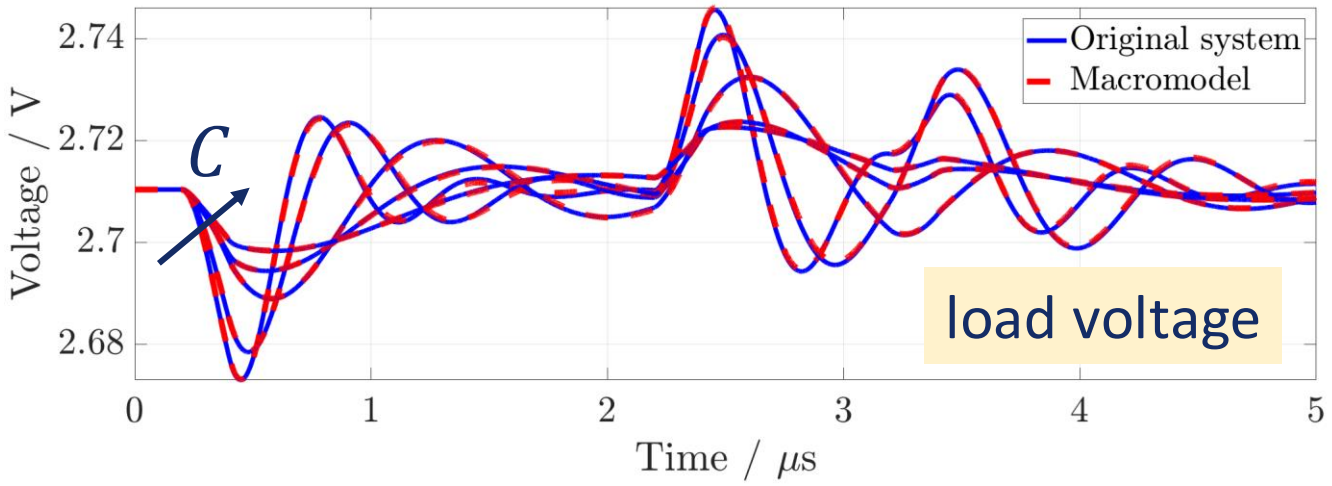
Rational model with poles:

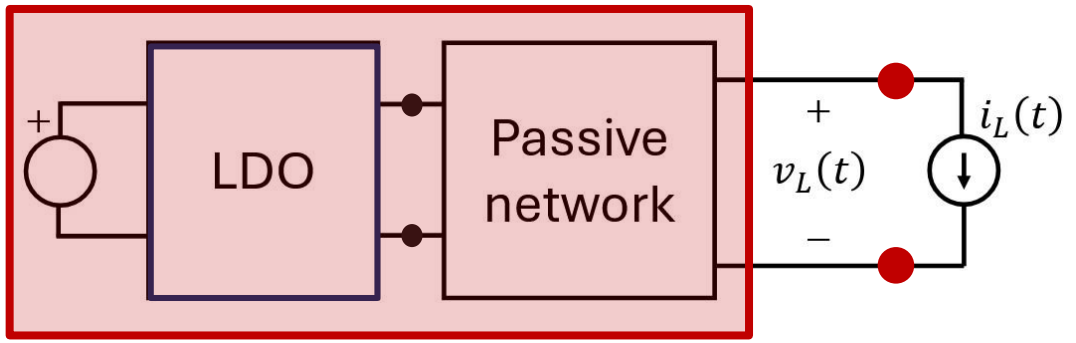
$\nu_1 = 8, \nu_2 = 8, \nu_3 = 5$

e) Application example: LDO regulator

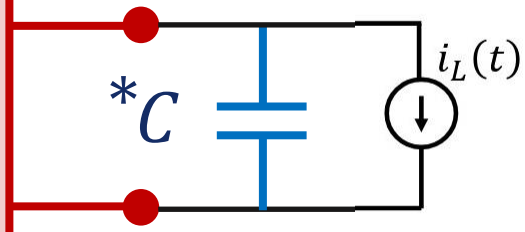
In time domain, with **external loads**







Nonlinear macromodel



Runtime (using HSPICE)

Original circuit: **5.36 s** **12X speedup!**

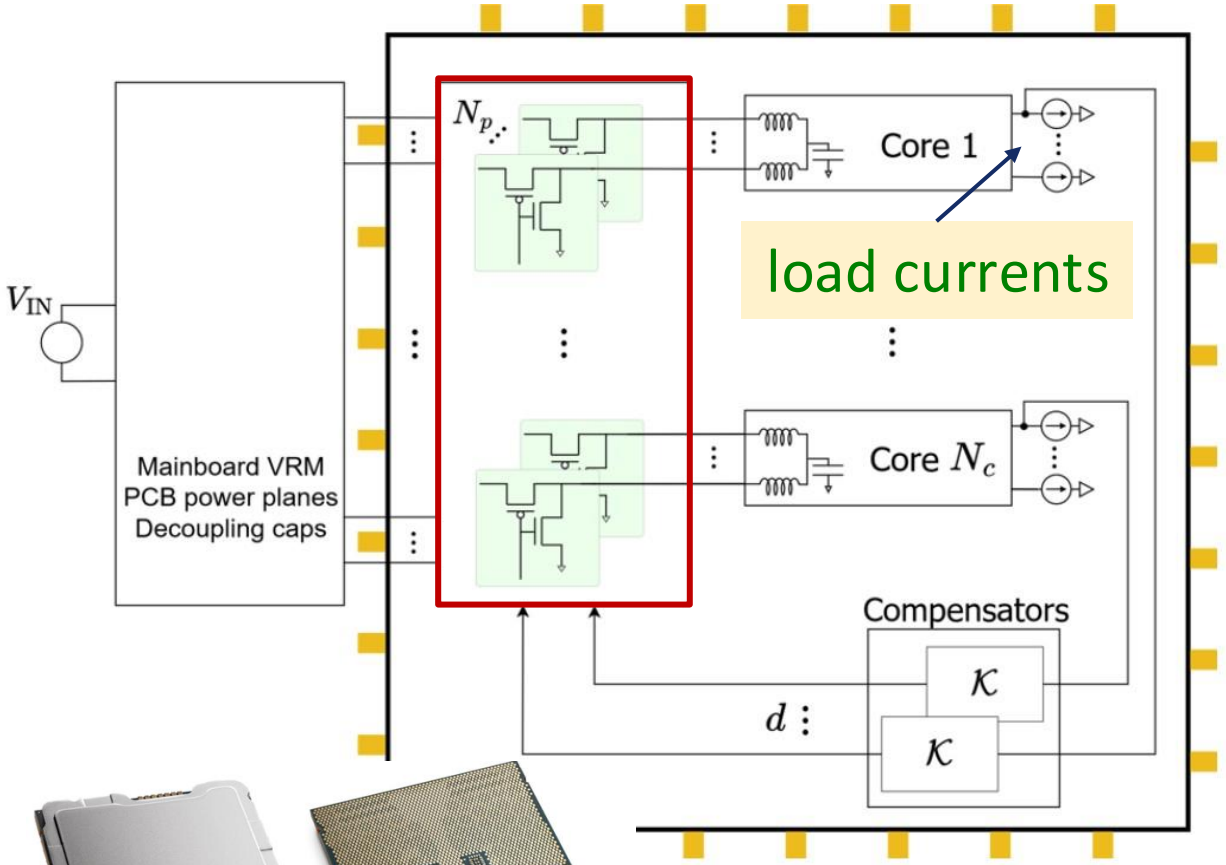
Bilinear macromodel: **0.45 s**

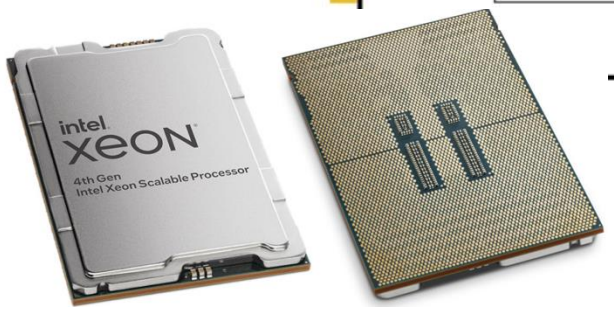
✓ Simulation using bilinear macromodel is **fast** and **accurate** for a range of loads

∗ capacitive load includes resistive parasitics (R-R-C), $C \in [1, 200]$ nF

e) Application example: PDN, integrated VRs

Microprocessor **PDN with Integrated Voltage Regulators** (switching)

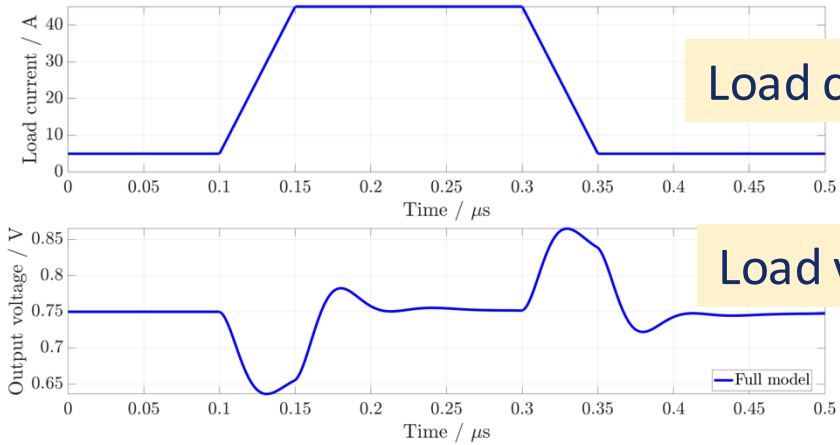




***courtesy of Intel**

Typical function

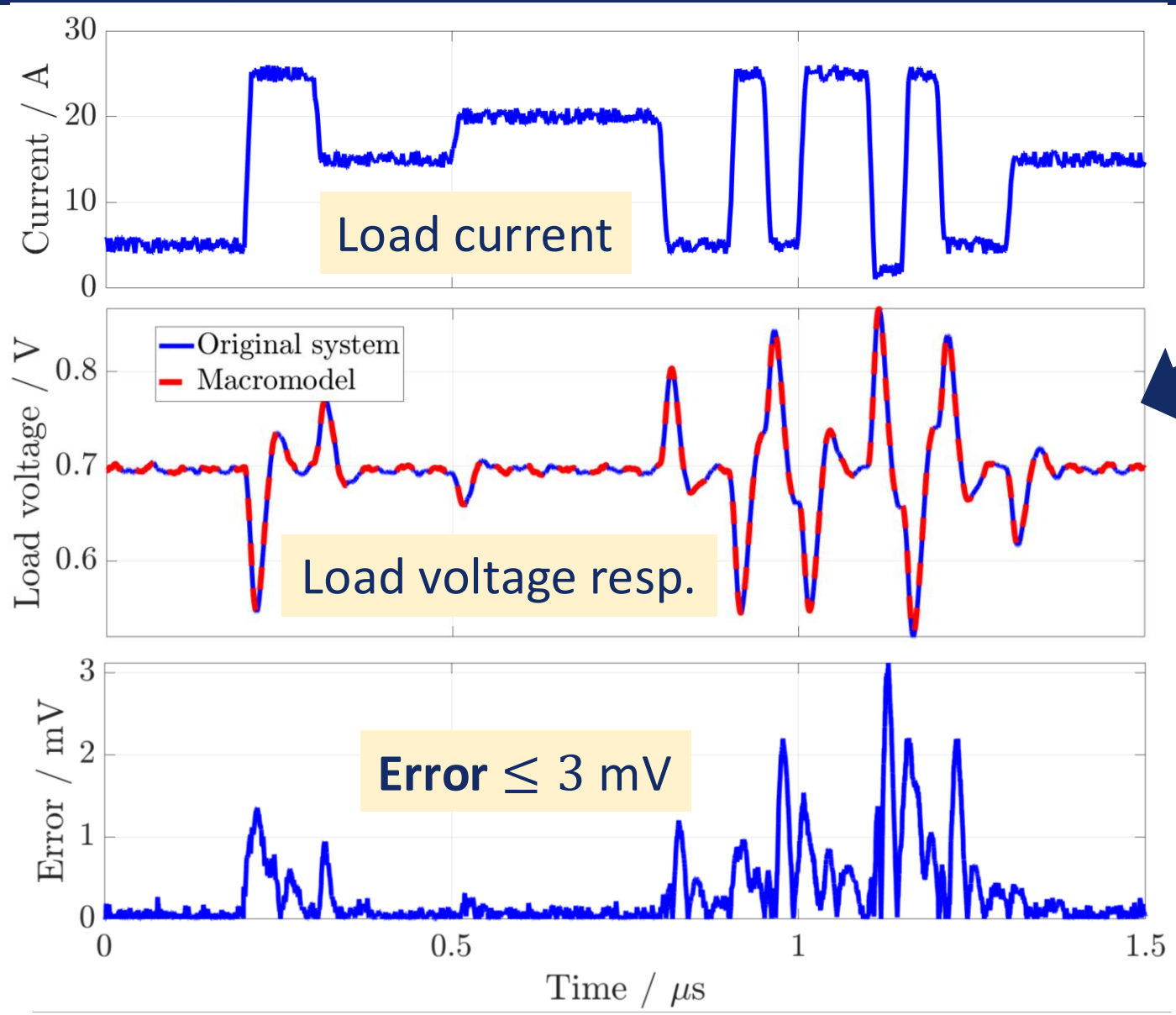
- **regulate load voltage** to constant $V_{\text{reference}}$
- **feedback control** of switching converters to reduce droop → nonlinearity!



Modeling assumptions

- averaged switch model
- consider only **one** load output

e) Application example: PDN, integrated VRs



- Quadratic model ($M = 2$) with $\nu_1 = \nu_2 = 9$ poles
- **Synthesized macromodel** is simulated in **HSPICE** and compared with original PDN

Runtime (HSPICE)

Original system: **1592 s**

Bilinear mod.: **2.46 s (650X speedup)**

✓ Bilinear macromodel provides **SPICE-compatible**, **accurate** and **faster** simulation

Summary

- Recent extensions in macromodeling technology from PoliTO
  - Not available in the market (yet)
- Parameterized modeling tool
  - Scalable macromodels, including dependence on several external parameters
  - Modeling tool available w GUI
  - Customization possible
- Application of parameterized modeling to small-signal models of NL ckts
  - Can be bias-dependent, any (smooth) parameter can be handled
  - Operating point may vary with time! Stability guaranteed!
- Extension to full PDN characterization and simulation, including FIVRs
  - Fast transient solvers enabled by large-scale (sparse, compressed) MOR
- Black-box nonlinear macromodeling
  - Application to voltage-regulated PDNs (both component and system level)

Macromodeling: what's next?